IN THE CLAIMS:

Claims 1-12, 15-34, 39-47, and 50-58 are pending. Please amend claims 1-3, 5, and 15 as follows:

1. (Currently amended) A memory device comprising a substrate, an insulating layer overlying the substrate, and an electrode structure, a charge storage node and a lamination structure overlying the insulating layer, the lamination structure including an insulating film and a semiconductor film, the lamination structure being disposed between the electrode structure and the charge storing node, the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing in the second configuration from the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge is stored on the node in the first configuration.

2. (Currently amended) A memory device according to claim 1, wherein the memory device has a control electrode[[,]] operable to change the energy band profile ~~being changed~~ between the first and the second configuration. ~~in response to a voltage supplied to the control electrode.~~

3. (Currently amended) A memory device comprising:

a path for charge carriers;

a charge storing node to produce a field which alters a conductivity of the path;

an insulating layer between the path and the charge storing node;

an electrode structure; and

a lamination structure including an insulating film and a semiconductor film,

the lamination structure being disposed between [[an]] the electrode structure and the charge storing node,

the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing in the second configuration between the electrode structure and the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge on the node is stored in the first configuration.

4. (Original) A memory device according to claim 3, wherein the memory device has a control electrode, the energy band profile being changed between the first configuration and the second configuration in response to a voltage supplied to the control electrode.

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5. (Currently amended) A memory device comprising:

a substrate;

a source-drain path in the substrate for charge carriers;

an insulating layer over the source drain path;

a charge storing node over the insulating layer to produce a field which alters a conductivity of the source-drain path;

an electrode structure; and

a lamination structure including an insulating film and a semiconductor film,

the lamination structure being disposed between the electrode structure and the charge storing node,

the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing in the second configuration from the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge on the node is stored in the first configuration.

6. (Original) A memory device according to claim 5 wherein the memory device has a control electrode, the energy band profile being changed between the first configuration and the second configuration in response to a voltage supplied to the control electrode.

7. (Original) A memory device according to claim 5 wherein the insulating film and the conductive film of the lamination structure are formed of silicon nitride and silicon material, respectively.

8. (Original) A memory device according to claim 7 wherein the lamination structure further includes another film of silicon nitride, the silicon material being disposed between the silicon film and the other silicon nitride film.

9. (Original) A memory device according to claim 7 wherein the lamination structure further includes another film of silicon material, the silicon nitride film being disposed between the film of silicon material and the other film of silicon material.

10. (Original) A memory device according to claim 7 wherein the silicon material comprises polysilicon.

11. (Original) A memory device according to claim 8 wherein the silicon material comprises polysilicon.

12. (Original) A memory device according to claim 9 wherein the silicon material comprises polysilicon.

13-14. (Cancelled)

15. (Currently amended) A memory device comprising:

a substrate;

a charge storage node,

an insulating layer between the charge storage node and the substrate;

an electrode structure, and

a barrier structure between the electrode structure and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable by an external bias to provide selectively a relatively low barrier height for which charge carriers can pass from the electrode structure to the charge storage node and vice versa to charge and discharge the node, and a relatively high barrier height to store charge carriers on the charge storage node.

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16. (Original) A memory device according to claim 15 wherein the barrier structure includes a region of barrier material providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential.

17. (Original) A memory device according to claim 16 wherein the height of said barrier component is raised and lowered in response to raising and lowering of the height of the barrier provided by the variable internal electrostatic barrier potential.

18. (Original) A memory device according to claim 16 wherein the region of barrier material is formed of a material selected from the group consisting of silicon dioxide and silicon nitride.

19. (Original) A memory device according to claim 16 including a further said region of barrier material providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential.

20. (Original) A memory device according to claim 1 including a gate to receive said external bias to configure the barrier between said high and low barrier heights.

21. (Previously amended) A memory device comprising:

a substrate;

an array of memory cells configured on the substrate; and

a plurality of word lines and data lines extending between the cells, the word lines being operable to receive cell selection signals;

each of the memory cells comprising a charge storage node, an electrode forming part of one of the data lines, and a barrier structure between the electrode and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node for charging and discharging the node, and a relatively high barrier height to store charge carriers on the charge storage node.

22. (Original) A memory device according to claim 21 wherein each of the memory cells includes a source-drain path with a conductivity which is altered as a function of the charge stored on the charge storage node, and the device further including a plurality of sense lines coupled to the source drain paths of the cells, and refreshing circuitry responsive to the sense lines to refresh data on the data lines.

23. (Original) A memory device according to claim 15 wherein the barrier structure is formed of crystalline material.

24. (Original) A memory device according to claim 15 wherein the barrier structure includes polycrystalline silicon.

25. (Original) A memory device according to claim 15 including a gate to apply said external bias to the barrier structure.

26. (Original) A memory device according to claim 15 including a substrate and configured so that the charge storage node is formed overlying the substrate, the barrier structure overlies the charge storage node, and the electrode structure overlies the barrier structure.

27. (Original) A memory device according to claim 26 including an insulating layer overlying the substrate, the charge storage node, barrier structure and the electrode structure overlying the insulating layer.

28. (Original) A memory device according to claim 27 including further device features formed in the substrate, the further device features underlying the insulating layer.

29. (Original) A memory device according to claim 27 wherein the insulating layer comprises an oxide of the material of the substrate.

30. (Original) A memory device according to claim 27 wherein the insulating layer extends over side edges of the barrier structure and the charge storage node.

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31. (Original) A memory device according to claim 26 wherein the barrier structure is substantially co-extensive with the charge storage node.

32. (Original) A memory device according to claim 15 wherein the barrier structure has a material composition that provides an internal relatively high internal electrostatic barrier in the absence of an applied voltage to the electrode structure, whereby the electrostatic barrier can be lowered upon application of the external bias to the electrode structure.

33. (Original) A memory device according to claim 27 including a gate configured to apply said external bias into the barrier structure selectively to control conduction of charge carriers between the electrode structure and the charge storage node.

34. (Original) A memory device according to claim 15 wherein the charge storage node is made of conductive silicon material.

35-38. (Cancelled)

39. (Original) A device according to claim 21 including refresh circuitry to refresh the level of charge stored on the charge storage nodes individually.

40. (Original) A device according to claim 21 including reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually.

41. (Original) A device according to claim 21 including writing circuitry to write charge to the charge storage nodes of the cells individually.

42. (Original) A memory device according to claim 21 wherein the barrier structure is formed of crystalline material.

43. (Original) A memory device according to claim 21 wherein the barrier structure includes polycrystalline silicon.

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44. (Original) A memory device according to claim 21 wherein each of the memory cells includes a gate to apply said external bias to the barrier structure.

45. (Previously amended) A memory device comprising

a substrate,

an array of memory cells configured on the substrate,

a plurality of word lines and data lines extending between the cells,

each of the memory cells comprising a charge storage node, an electrode structure coupled to one of the data lines and a barrier structure between the electrode structure and the charge storage node, the barrier structure providing an internal electrostatic barrier potential of a relatively high barrier height to store charge carriers on the charge storage node the barrier being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node,

reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually, and

writing circuitry to write charge onto the charge storage nodes of the cells individually.

46. (Original) A memory device according to claim 45 including an electrically insulating layer on the substrate with the array of memory cells overlying the insulating layer.

47. (Original) A memory device according to claim 45 wherein the substrate is comprised of silicon, the insulating layer is selected from a group comprising an oxide and a nitride of silicon, the charge storage node is formed of a conductive silicon material and the barrier structure is formed of polysilicon material.

48-49. (Cancelled).

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50. (Previously presented) A memory device comprising:

a substrate,

an array of memory cells configured on the substrate,

an electrically insulating layer on the substrate,

a plurality of word lines and data lines extending between the cells,

each of the memory cells comprising a barrier structure and a memory node, the barrier structure overlying the insulating layer and providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the barrier being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height whereby a current flows through the barrier structure to change the voltage on the memory node,

reading circuitry to read the level of charge stored on the memory nodes of the cells individually, and

writing circuitry to write charge onto the charge storage nodes of the cells individually.

51. (Previously presented) A memory device according to claim 50, wherein the substrate is comprised of silicon, the insulating layer is selected from a group comprising an oxide and a nitride of silicon.

52. (Previously presented) A memory device according to claim 50, wherein the memory node is formed of a conductive silicon material.

53. (Previously presented) A memory device according to claim 50, wherein the barrier structure is formed of polysilicon material.

54. (Previously presented) A memory device according to claim 50, including a control gate configured to control the barrier height presented by the barrier structure to a current that flows to and from the memory node.

55. (Previously presented) A memory device according to claim 50, wherein the current that flows to and from the memory node, flows vertically through the barrier structure.

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56. (Previously presented) A memory device comprising:

a substrate,

an array of memory cells configured on the substrate,

an electrically insulating layer on the substrate,

a plurality of word lines and data lines extending between the cells,

each of the memory cells comprising an electrode, a memory node, a barrier structure between the electrode and the memory node, and a control gate, the barrier structure overlying the insulating layer and providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate being operable to receive an external voltage bias applied to one of the word lines so as to apply a field to the barrier structure resulting in a relatively low barrier height whereby a current flows through between the electrode and the memory node through the barrier structure to change the voltage on the memory node, and

reading circuitry to read the level of charge stored on the memory nodes of the cells individually.

57. (Previously presented) A memory device comprising:

a substrate,

a horizontal transistor formed in the substrate, and

a vertically configured controllable conduction device overlying the horizontal transistor, comprising an electrode, a memory node, a barrier structure between the electrode and the memory node, and a control gate, the barrier structure providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate

being operable to receive an external voltage bias whereby the barrier structure presents a relatively low barrier height and a current flows between the electrode and the memory node through the barrier structure so as to change the voltage on the memory node.

58. (Previously presented) A method of fabricating a semiconductor device, comprising: providing a substrate, providing an electrically insulating layer on the substrate, fabricating an array of memory cells, providing a plurality of word lines and data lines extending between the cells, each of the memory cells comprising a barrier structure and a memory node, the barrier structure overlying the insulating layer and providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node the barrier being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height whereby a current flows through the barrier structure to change the voltage on the memory node, providing reading circuitry to read the level of charge stored on the memory nodes of the cells individually, and fabricating writing circuitry to write charge onto the charge storage nodes of the cells individually.